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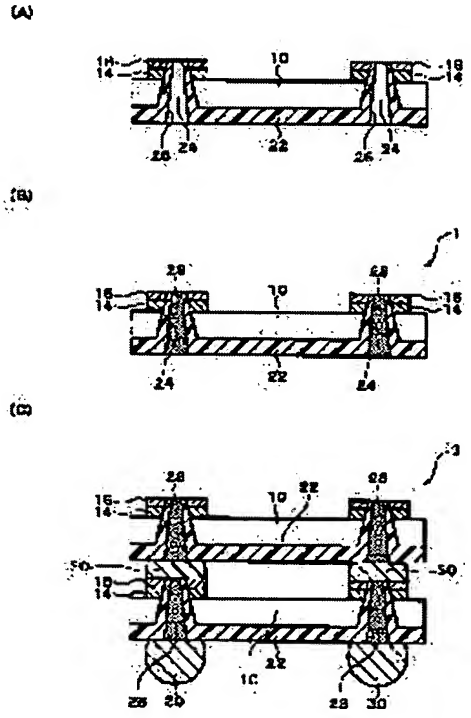
(54) SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC APPARATUS

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device and method of manufacturing the same, circuit board, and electronic apparatus, where electrical connections can be established easily with high reliability.

SOLUTION: The method of manufacturing the semiconductor device includes a first process of forming first through-holes 18 at, places where electrodes 14 are formed, in a semiconductor element 10 provided with the electrodes; a second process of providing an insulating material 22 in a region, including the inside parts of the first through-holes 18, so that second through holes 24 which pass through the insulating material 22 are formed; and a third process of providing a conductive member 28 inside the first through-holes 18 so that it passes through the second through-holes 24.



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* NOTICES *

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2.**** shows the word which can not be translated.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to electronic equipment at a semiconductor device and its manufacture method, and a circuit board list.
[0002]
[Background of the Invention] In recent years, the semiconductor device of the stack structure which accumulated two or more semiconductor chips is developed. Although the many carried out bonding of a wire or the lead to the electrode of a semiconductor chip and aimed at electric connection, since they prepared the wire etc., the limit was in the miniaturization.
[0003] that to which this invention solves this trouble -- it is -- the connection with that electric purpose -- high reliability -- with, it is in providing with electronic equipment the semiconductor device which can be planned easily and its manufacture method, and a circuit board list.
[0004]
[Means for Solving the Problem] (1) A manufacture method of a semiconductor device concerning this invention The 1st production process which forms the 1st through hole penetrated in a location of said electrode to a semiconductor device which has an electrode, The 2nd production process prepared in a field containing the inside of said 1st through hole so that it may have the 2nd through hole which penetrates said insulating material for an insulating material, and the 3rd production process which prepares a conductive member by the inside of said 1st through hole in the 2nd through hole which penetrates said insulating material at least are included.
[0005] According to this invention, electrical installation of one field of a semiconductor device and a field of another side is planned only by preparing a conductive member in the 2nd through hole of a semiconductor device. Since a conductive member is prepared in the 2nd through hole which penetrates an insulating material, it can aim at an insulation with a semiconductor device and a conductive member easily.
[0006] (2) In a manufacture method of this semiconductor device, you may carry out the laminating of two or more semiconductor devices manufactured by above-mentioned method, and may also include further a production process which connects said up-and-down semiconductor device electrically through said conductive member.
[0007] According to this, two or more semiconductor devices are electrically connected by conductive member which penetrates a semiconductor device. By this, it is the minimum magnitude, for example, a semiconductor device of three or more steps of stack structures can be manufactured easily.
[0008] (3) A manufacture method of a semiconductor device concerning this invention The 1st production process which forms the 1st through hole penetrated in a location of said electrode to the 1st and 2nd semiconductor devices which have an electrode, The 2nd production process prepared in a field containing the inside of said 1st through hole so that it may have the 2nd through hole which penetrates said insulating material for an insulating material, While connecting electrically, preparing a conductive member in said electrode of said 1st semiconductor device and inserting said conductive member in said 2nd through hole in said 2nd semiconductor device, the 3rd production process which accumulates said 1st and 2nd semiconductor devices is included.
[0009] According to this invention, while assembling two or more semiconductor devices to a laminated structure, an electric flow of both sides of each semiconductor device can be aimed at. Therefore, simplification of a manufacturing process can be attained. Since a conductive member is prepared in the 2nd through hole which penetrates an insulating material, it can aim at an insulation with a semiconductor device and a conductive member easily.
[0010] (4) In a manufacture method of this semiconductor device, a field opposite to a field in which said electrode in said semiconductor device was formed in said insulating material may be covered and established at said 2nd production process.

[0011] According to this, since what is necessary is to cover a field of a semiconductor device and just to prepare an insulating material, it can prepare easily. Moreover, a semiconductor device can be made easy to deal with it in a subsequent production process, when especially a semiconductor device is thin. Furthermore, for example, an insulating material can raise the reliability of a semiconductor device in a final product in the middle of manufacture by using it as a stress relaxation layer of a semiconductor device.
[0012] (5) In a manufacture method of this semiconductor device, said insulating material may connect said conductive member and said electrode electrically by consisting of resin, heating [said two or more semiconductor devices] lamination and said resin for said resin as adhesives, and making hardening contraction of said resin complete.
[0013] According to this, since it not only uses resin as adhesives, but electrical installation of an up-and-down semiconductor device can be performed using hardening contraction of resin, simplification of a production process can be attained.
[0014] (6) Before sticking said two or more semiconductor devices, said resin may be heated and that adhesive strength may be made to discover in a manufacture method of this semiconductor device.
[0015] (7) In a manufacture method of this semiconductor device, said insulating material consists of resin, is said 2nd production process, and may apply and prepare said resin.
[0016] Since an insulating material is prepared only by applying resin according to this, handling of a semiconductor device is easy. That is, an insulating material can be formed, without using special equipment. Therefore, an insulating material can be easily formed in low cost and a short time.
[0017] (8) In a manufacture method of this semiconductor device, said 1st through hole may be buried at said 2nd production process, said insulating material may be prepared at it, and said 2nd through hole may be formed so that said insulating material may be penetrated with a path smaller than said 1st through hole inside said 1st through hole.
[0018] Thus, by forming an insulating material, a semiconductor device and a conductive member can be insulated certainly. That is, double-sided electrical installation can be planned, without making a semiconductor device short-circuit electrically.
[0019] (9) Said conductive member is conductive paste, is said 3rd production process, and may make said 2nd through hole fill up with said conductive paste in a manufacture method of this semiconductor device.
[0020] Since according to this you make it filled up with the 2nd through hole and conductive paste is prepared, electrical installation can be planned to both sides, without reducing a mechanical strength of a semiconductor device.
[0021] (10) In a manufacture method of this semiconductor device, said conductive member is a bump, is said 3rd production process, and may also insert said some of bumps [at least] in said 2nd through hole in said 2nd semiconductor device.
[0022] According to this, a conductive member can be certainly prepared in the 2nd through hole.
[0023] (11) In a manufacture method of this semiconductor device, plurality may carry out the laminating of said bump.
[0024] (12) Melting of said bump may be carried out and said 2nd through hole may be made filled up with her after said 3rd production process in a manufacture method of this semiconductor device.
[0025] According to this, since it is filled up with the 2nd through hole, a mechanical strength of a semiconductor device can be raised.
[0026] (13) In a manufacture method of this semiconductor device, a taper which becomes small may be attached and formed as said electrode of said semiconductor device is approached in said 2nd through hole.
[0027] According to this, a solid conductive member can be made easy to insert in the 2nd through hole, for example.
[0028] (14) In a manufacture method of this semiconductor device, a taper which becomes small may be attached and formed as said 2nd through hole is separated from said electrode of said semiconductor device.
[0029] According to this, an omission stop of a conductive member prepared in the 2nd through hole can be planned.
[0030] (15) a manufacture method of this semiconductor device -- setting -- said 1st through hole or said 2nd through hole -- either may be formed by laser beam at least.
[0031] According to this, a thin hole can be easily formed in a semiconductor device. Therefore, even if an appearance of an electrode of a semiconductor device is small, a through hole which penetrates a semiconductor device can be certainly formed in a location of an electrode.
[0032] (16) In a manufacture method of this semiconductor device, said laser beam may be irradiated from a field opposite to a field in which said electrode of said semiconductor device was formed.
[0033] According to this, a sediment produced by use of a laser beam is made that it is hard to make an electrode accumulate. Therefore, a through hole can be formed easily and a reliable semiconductor device can be formed.
[0034] (17) It comes to manufacture a semiconductor device concerning this invention by the manufacture method of the above-mentioned semiconductor device.

[0035] (18) A semiconductor device concerning this invention has an electrode, and contains a semiconductor device by which a through hole was formed in a location of said electrode, an insulating material prepared in a field including an inside of said through hole, and a conductive member prepared so that it might pass along a medial axis of said through hole.
[0036] According to this invention, one field of a semiconductor device and a field of another side are electrically connected by conductive member prepared in a through hole. In the interior of a semiconductor device, since a flow of both sides is achieved, a small semiconductor device can be offered.
[0037] (19) In this semiconductor device, said conductive member buries said through hole, and may be prepared.
[0038] According to this, a mechanical strength of a semiconductor device is not reduced.
[0039] (20) In this semiconductor device, a taper which becomes small may be attached as said through hole approaches said electrode of said semiconductor device.
[0040] (21) In this semiconductor device, a taper which becomes small may be attached as said through hole separates from said electrode of said semiconductor device.
[0041] According to this, an omission stop of a conductive member prepared in a through hole can be planned.
[0042] (22) In this semiconductor device, said insulating material covers a field opposite to a field in which said electrode in said semiconductor device was formed, and may be prepared while exposing said conductive member.
[0043] According to this, stress applied to a semiconductor device can be eased, for example. Therefore, a reliable semiconductor device can be offered.
[0044] (23) In this semiconductor device, said conductive member may be projected on the outside of said through hole in a part in the opposite side with a field in which said electrode in said semiconductor device was formed.
[0045] According to this, when carrying out a laminating to other semiconductor devices, alignment of a semiconductor device becomes easy on the basis of a projecting portion.
[0046] (24) In this semiconductor device, the laminating of the above-mentioned semiconductor device may be carried out, and said up-and-down semiconductor device may be electrically connected by said conductive member.
[0047] (25) As for the circuit board concerning this invention, the above-mentioned semiconductor device is carried.
[0048] (26) Electronic equipment concerning this invention has the above-mentioned semiconductor device.
[0049]
[Embodiment of the Invention] Hereafter, the gestalt of suitable operation of this invention is explained with reference to a drawing. However, this invention is not limited to the gestalt of the following operations. In addition, the contents shown in the gestalt of operation shown below are applicable as much as possible also in the gestalt of other operations.
[0050] (Gestalt of the 1st operation) Drawing 1 (A) - drawing 2 (C) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 1st operation which applied this invention. Drawing 1 (A) is drawing showing the semiconductor chip 10 (semiconductor device) used with the gestalt of this operation. In the example shown in the gestalt of this operation, the semiconductor chip 10 which comes to carry out **** cutting of the semiconductor wafer at plurality is used. Although a semiconductor chip 10 is generally a rectangular parallelepiped (a cube is included), the configuration may not be limited but may be spherical.
[0051] Grinding of the semiconductor chip 10 may be thinly carried out to the thickness of the semiconductor chip 12 (or semiconductor wafer) of a basis. In detail, grinding of the field where a semiconductor chip 10 is opposite to the field (active side) in which the integrated circuit was formed is carried out. Thickness of a semiconductor chip 10 can be made as thin as possible if it can leave the portion in which the integrated circuit was formed. Although the thickness is not limited, you may be about 50 micrometers. By using the thin semiconductor chip 10, the semiconductor device of small and high density can be manufactured.
[0052] Grinding of a semiconductor chip 10 may be performed after carrying out before carrying out the dicing of the semiconductor wafer, or carrying out dicing. Moreover, the slot of the depth more than the thickness of a semiconductor chip 10 is beforehand formed in the semiconductor wafer, and the method of dividing into two or more thin semiconductor chips 10 may be applied by carrying out grinding of the semiconductor wafer 12.
[0053] A semiconductor chip 10 has two or more electrodes 14 in the near field in which the integrated circuit was formed. Although an electrode 14 has common aluminum, it may be formed from copper etc. An electrode 14 may make the square shape whose one side is about 100 micrometers, for example, although the magnitude differs according to layout. An electrode 14 is formed in the edge or center section of the semiconductor chip 10. An electrode 14 may be formed together with two sides of a semiconductor chip 10, or four sides.
[0054] The center section of the electrode 14 is avoided in a semiconductor chip 10, an edge is covered to it, and a passivation film (not shown) is formed in it in many cases. A passivation film can be formed with SiO2, SiN, or polyimide resin.

[0055] Plating 16 may be formed on an electrode 14. The production process which forms plating 16 may be the back before carrying out grinding of the semiconductor chip 12. Plating 16 may be formed by electroless deposition. By forming plating 16 on an electrode 14, the oxide film of an electrode 14 is removable. Furthermore, it can be made easy to get wet the pewter formed at a next production process by plating 16. It opts for plating 16 with the material of an electrode 14. When an electrode 14 is aluminum, plating 16 may be formed from the material containing nickel and gold.

[0056] The manufacture method of the semiconductor device concerning the gestalt of this operation performs the following production processes using the above-mentioned semiconductor chip 10. Or this manufacture method may also include either of the above-mentioned production processes further.

[0057] As shown in drawing 1 (B), the 1st through hole 18 is formed in the above-mentioned semiconductor chip 10. The 1st through hole 18 penetrates a semiconductor chip 10 in the location of each electrode 14. The 1st through hole 18 may be formed using laser (for example, an YAG laser and excimer laser). If laser is used, even if one side of an electrode 14 is the square shape which is about 100 micrometers, the 1st through hole 18 which has a path smaller than it can be easily formed in the field inside an electrode 14, for example. In addition, in plane view, the 1st through hole 18 may be any of circular or a square shape, and may be other configurations.

[0058] A laser beam may be irradiated only from one field of a semiconductor chip 10, or may glare from both sides (or simultaneous [Sequence]). In the case of the former, a laser beam may be irradiated from a field opposite to the field in which the electrode 14 of a semiconductor chip 10 was formed. According to this, it can do that it is hard to make the sediment produced by use of a laser beam deposit on an electrode 14 (plating 16). Moreover, the sediment which forms a wrap protective coat (not shown) and produces an electrode 14 (plating 16) by use of a laser beam may be made to deposit on the protective coat beforehand. If the protective coat on an electrode 14 (plating 16) is removed behind according to this, it is not necessary to make an electrode 14 (plating 16) deposit an excessive thing. Protective coats may be a resist, ink, etc. In addition, when irradiating a laser beam, a hollow (not shown) may be formed beforehand and a laser beam may be irradiated by considering it as a mark.

[0059] The inside of the 1st through hole 18 may be formed in the shape of a taper. For example, the 1st through hole 18 may attach and form the taper 20 which becomes small as it approaches the electrode 14 of a semiconductor chip 10. In this case, the major diameter of the 1st through hole 18 may be the magnitude within 2 double to the thickness of a semiconductor chip 10. According to this, it is easy to form the taper-like 1st through hole 18 by the laser beam. For example, when the thickness of a semiconductor chip 10 is about 50 micrometers, the major diameter of the 1st through hole 18 may be formed in about 60-80 micrometers, and a minor diameter may be formed in about 30-40 micrometers. By attaching such a taper 20, the same taper 26 (refer to drawing 2 (A)) as the 2nd through hole 24 can be attached at a next production process. Or the 1st through hole 18 may make a perpendicular internal surface to the field of a semiconductor chip 10.

[0060] These production processes may be performed sticking two or more semiconductor chips 10 on the dicing tape used at the time of grinding. According to this, a laser beam can be irradiated in an exact location on the basis of the dicing line where two or more semiconductor chips 10 come to stand in a line.

[0061] As shown in drawing 1 (C), an insulating material 22 is formed in the field containing the inside of the 1st through hole 18. The 1st through hole 18 may be buried and an insulating material 22 may be formed so that it may illustrate. According to this, a semiconductor chip 10 can be certainly insulated in the 1st through hole 18. Or an insulating material 22 may be formed only in the internal surface of the 1st through hole 18. In addition, an insulating material 22 can be formed by resin, the oxide film, or the nitride.

[0062] A field opposite to the field in which the electrode 14 in a semiconductor chip 10 was formed in the insulating material 22 may be covered and established so that it may illustrate. On extension of the direction where the 1st through hole 18 is prolonged, an insulating material 22 may be formed further. In this case, on a semiconductor chip 10, an insulating material 22 may be formed so that it may become flat-tapped. According to this, since what is necessary is just to form an insulating material 22 all over a semiconductor chip 10, it can be easily prepared inside the 1st through hole 18. Moreover, a semiconductor chip 10 can be made easy to prevent a crack and the crack of the cone semiconductor chip 10 thinly, and to deal with it in a subsequent production process. Furthermore, even if a semiconductor chip 10 expands with the heat at the time of grinding and it will be in curvature or a cone condition, the curvature is absorbable with an insulating material 22. That is, the stress applied to a semiconductor chip 10 can be eased by the insulating material 22.

[0063] An insulating material 22 may be formed by applying. In this case, an insulating material 22 may be resin. What is necessary is just to apply resin using a dispenser. Resin is made that it is easy to make a semiconductor chip 10 cover with flying a solvent and making it dry. According to this, since resin is only applied, the handling of a semiconductor chip 10 is easy. When using a crack and the cone semiconductor chip 10 thinly, especially since it is not necessary to

break a semiconductor chip 10, it is effective.
[0064] Or an insulating material 22 may be formed using screen-stencil or an ink jet printer method. It is possible to apply a high speed and ink economically without futility especially by applying the technology put in practical use for ink jet printers according to the ink jet printer method. The ink jet arm head which is not illustrated was put in practical use for example, for ink jet printers, the piezo jet type using a piezoelectric device or its bubble jet (registered trademark) type using the electric thermal-conversion object as an energy generation element is usable, and regurgitation area and a regurgitation pattern can be set as arbitration.
[0065] In addition, an insulating material 22 may be formed with chemical vapor deposition (CVD) or a photopolymer using a mask, and the means is not limited.
[0066] As shown in drawing 2 (A), the 2nd through hole 24 is formed. After burying the 1st through hole 18 at an above-mentioned production process and forming an insulating material 22 at it, the 2nd through hole 24 may be formed. The 2nd through hole 24 is formed with a path smaller than the 1st through hole 18 inside the 1st through hole 18. The 2nd through hole 24 penetrates an insulating material 22. When an insulating material 22 is formed until it results on the field of a semiconductor chip 10 so that it may illustrate, the 2nd through hole 24 penetrates further the portion of the insulating material 22 prepared on extension of the 1st through hole 18.
[0067] The contents explaining the 1st through hole 18 are applicable to the formation method of the 2nd through hole 24. That is, a laser beam is irradiated and the 2nd through hole 24 may be formed. According to this, since a thin through hole can be formed, the 2nd through hole 24 which has a path still smaller than the path of the 1st through hole 18 can be formed easily.
[0068] The inside of the 2nd through hole 24 may be formed in the shape of a taper. For example, the 2nd through hole 24 may attach and form the taper 26 which becomes small as it approaches the electrode 14 of a semiconductor chip 10. A solid conductive member can be made easy to insert in from the opposite side with the field in which the electrode 14 of a semiconductor chip 10 was formed, for example according to this. The 2nd through hole 24 can determine the magnitude of a path in the range that what is necessary is just to be able to penetrate an insulating material 22, covering a semiconductor chip 10 by the insulating material 22 in the inside. In addition, the shape of a plan type of the 2nd through hole 24 is not limited.
[0069] Or the inside of the 2nd through hole 24 may make a perpendicular internal surface to the field of a semiconductor chip 10.
[0070] As shown in drawing 2 (B), a conductive member 28 is formed inside the 2nd through hole 24. A conductive member 28 is formed in the 2nd through hole 24 at least. A conductive member 28 may be formed so that it may pass along the medial axis of the 2nd through hole 24. Or it shifts from a medial axis and a conductive member 28 may be formed, as long as it can aim at the insulation with a semiconductor chip 10 through an insulating material 22. The 2nd through hole 24 may be made to fill up with a conductive member 28 so that it may illustrate. A conductive member 28 may be conductive paste. As conductive paste, low material, such as conductive resin or a pewter, may be used. Electrical installation can be planned to both sides of a semiconductor chip 10 by burying the 2nd through hole 24 and forming a conductive member 28, without reducing the mechanical strength of a semiconductor chip 10.
[0071] Or it prepares so that it may pass along the medial axis of the hole (the 2nd through hole) surrounded by the insulating material 22 by the inside of the 1st through hole 18 in the conductive member 28 by the above-mentioned production process, when an insulating material 22 is formed only in the internal surface of the 1st through hole 18. Even in this case, a hole may be made to fill up with conductive paste.
[0072] According to the above production process, the semiconductor device 1 shown in drawing 2 (B) is obtained. A semiconductor device 1 has an electrode 14 and contains the semiconductor chip 10 with which the through hole (for example, the 2nd through hole 24) was formed in the location of an electrode 14, an insulating material 22, and a conductive member 28.
[0073] In the example to illustrate, the insulating material 22 is formed in the field including the inside of the 2nd through hole 24. In other words, the 2nd through hole 24 is surrounded and formed by the insulating material 22. Moreover, an insulating material 22 covers a field opposite to the field in which the electrode 14 of a semiconductor chip 10 was formed, and may be prepared. According to this, the stress applied to a semiconductor chip 10 can be eased.
[0074] A conductive member 28 is formed so that it may pass along the medial axis of the 2nd through hole 24. A conductive member 28 buries the 2nd through hole 24, and may be prepared. According to this, since the 2nd through hole 24 is buried, the mechanical strength of a semiconductor chip 10 is not reduced. A conductive member 28 is exposed from the field of an insulating material 22 or a semiconductor chip 10 in the opposite side with the field in which the electrode 14 of a semiconductor chip 10 was formed. And a taper 26 may be attached as mentioned above and, as for the 2nd through hole 24, the side of a conductive member 28 may be formed in the shape of a taper

corresponding to this. In addition, the configuration of others of a semiconductor device is as having indicated the manufacture method.

[0075] According to the semiconductor device in the gestalt of this operation, one field of a semiconductor chip 10 and the field of another side are electrically connected by the conductive member 28 prepared in the through hole (for example, the 2nd through hole 24). In the interior of a semiconductor chip 10, since a flow of both sides is achieved, a small semiconductor device can be offered.

[0076] As shown in drawing 2 (C), the laminating of two or more semiconductor chips 10 (semiconductor device 1) formed by the above-mentioned method is carried out. In detail, the up-and-down semiconductor chip 10 is electrically connected through a conductive member 28. That is, the semiconductor device of stack structure is manufactured. A field opposite to the field in which the electrode 14 of one semiconductor chip 10 was formed may be made to counter the field in which the electrode 14 of the semiconductor chip 10 of another side was formed, and the laminating of the up-and-down semiconductor chip 10 may be carried out so that it may illustrate. Or the fields in which the electrode 14 was formed may be made to counter, fields opposite to it may be made to counter, and the laminating of the three or more semiconductor chips 10 may be carried out combining these.

[0077] The up-and-down semiconductor chip 10 may be electrically connected with a pewter 30. What is necessary is just to form a pewter 30 in the semiconductor chip 10 of either or both beforehand. A pewter 30 may be made into the shape of a ball, and may be carried, or may be prepared between the up-and-down semiconductor chips 10 with the surface tension at the time of melting.

[0078] A pewter 30 is joined to the conductive member 28 of other semiconductor chips 10 on the electrode 14 (plating 16) of a semiconductor chip 10. Here, a pewter 30 connects electrically the conductive member 28 in the semiconductor chip 10 of the side prepared on the electrode 14 (plating 16) insulated with the electrode 14 by the insulating material 22 while connecting the up-and-down semiconductor chip 10. That is, in the semiconductor chip 10 of the side prepared on the electrode 14 (plating 16), it is [electrical installation / of an electrode 14 and a conductive member 28] good for the up-and-down laminating and the coincidence of a semiconductor chip 10 in drawing. According to this, simplification of a manufacturing process can be attained. Or before carrying out a laminating, in one semiconductor chip 10, an electrode 14 and a conductive member 28 may be connected electrically beforehand. In this case, if the electrical conducting material (for example, conductive paste) which is not illustrated is prepared so that an electrode 14 (plating 16) and a conductive member 28 may be covered, both electrical installation can be planned. In the example to illustrate, an electrode 14 and a conductive member 28 are electrically connected by the electrical conducting material with which a **** does not illustrate the semiconductor chip 10 of the maximum upper layer.

[0079] In addition, the topology of the up-and-down semiconductor chip 10 may apply which gestalten, such as metal cementation by the electric conduction resin paste (an anisotropy electrical conducting material is included), Au-Au, or Au-Sn, or cementation by the shrinkage force of insulating resin, besides a pewter 30. For example, when aiming at metal cementation, it may connect with the conductive member 28 of a field opposite to the field in which the electrode 14 of a semiconductor chip 10 was formed, a bump may be prepared, and you may make it join on the electrode 14 (plating 16) of other semiconductor chips 10.

[0080] A pewter 30 may be formed in a field opposite to the field which turns [semiconductor chip / 10 / of the lowest layer] to other semiconductor chips 10. A pewter 30 may be made into the shape of a ball as mentioned above, and may be prepared. A pewter 30 may be formed in a field opposite to the field in which the electrode 14 of a semiconductor chip 10 was formed so that it may illustrate, or it may form an electrode 14 in the field to turn to. By forming a pewter 30 in the semiconductor chip 10 of the lowest layer, it can mount in the substrate (INTAPOZA) for mounting in the circuit board (mother board) or the circuit board easily.

[0081] Or when mounted in the circuit board, without forming a pewter 30 in the shape of a ball at the semiconductor chip 10 of the lowest layer, a pewter cream is applied to the circuit pattern by the side of the circuit board, and it is [electrical installation] good in drawing at the surface tension at the time of the melting. In addition, the field in which the electrode 14 was formed may counter the circuit board, and, as for the semiconductor chip 10 of the lowest layer, a field opposite to it may counter. In addition, the gestalt of the electrical installation of a semiconductor device and the circuit board may apply the gestalt of a publication until now.

[0082] According to the gestalt of this operation, electrical installation of one field of a semiconductor chip 10 and the field of another side is planned only by forming a conductive member 28 in the 2nd through hole 24 of a semiconductor chip 10. A conductive member 28 can aim at a flow with an electrode 14 certainly, if it prepares so that it may pass along the medial axis of the 2nd through hole 24 surrounded by the insulating material 22. Moreover, by the conductive member 28 which penetrates a semiconductor chip 10, by carrying out the laminating of two or more semiconductor devices, it is the minimum magnitude, for example, the semiconductor device of three or more steps of

stack structures can be manufactured easily.
[0083] Drawing 3 is drawing explaining the manufacture method of the semiconductor device concerning the modification of the gestalt of this operation. In this modification, an insulating material 22 is used as adhesives and the up-and-down semiconductor chip 10 is stuck. An insulating material 22 may be resin. As for resin, it is desirable that it is thermosetting resin. Resin is prepared in a field opposite to the field in which the electrode 14 in a semiconductor chip 10 was formed.
[0084] First, before accumulating two or more semiconductor chips 10, resin is heated and the adhesive strength is made to discover. In other words, resin is heated to the degree which will be in the condition (semi-hardening condition) that hardening is not completed. The up-and-down semiconductor chip 10 can be stuck by using as adhesives the resin prepared in the field of a semiconductor chip 10 by this.
[0085] And while carrying out the laminating of two or more semiconductor chips 10, the up-and-down semiconductor chip 10 is pasted up with the resin prepared in one semiconductor chip 10. That is, between the up-and-down semiconductor chips 10, resin is stuck to the field of each semiconductor chip 10, and is prepared. According to this, since between each semiconductor chip 10 is filled with resin, the stress (thermal stress etc.) applied to a semiconductor device can be eased.
[0086] Resin is heated and stiffened after sticking the up-and-down semiconductor chip 10. In detail, the resin which was in the semi-hardening condition when sticking the up-and-down semiconductor chip 10 is heated to the degree which will be in the condition that the hardening is completed. In this case, hardening contraction of the resin may be carried out. That is, the up-and-down semiconductor chip 10 is stuck by carrying out hardening contraction of the resin adhered to the field of each semiconductor chip 10. According to this, the conductive member 28 (pewter 30) of one semiconductor chip 10 and the electrode 14 (plating 16) of the semiconductor chip 10 of another side are mechanically connectable with the shrinkage force of resin. That is, it is not necessary to turn a semiconductor chip 10 to other semiconductor chips 10, and to press it anew. Therefore, simplification of a manufacturing process can be attained.
[0087] In addition, the resin used as adhesives may be prepared at another production process in the above-mentioned insulating member 22. That is, resin may be prepared in a field opposite to the field in which the electrode 14 in a semiconductor chip 10 was formed independently [the insulating member 22 prepared inside the 1st through hole 18].

[0088] Although the resin used as adhesives showed the example which fills between the up-and-down semiconductor chips 10 in this modification, after carrying out the laminating of the up-and-down semiconductor chip 10, the method of pouring in resin among both may be applied. Even in this case, you can make it filled up with resin between the up-and-down semiconductor chips 10, and the stress (thermal stress etc.) applied to a semiconductor device can be eased.
[0089] The gestalt is as a publication already including the resin (insulating material 22) with which the semiconductor device 4 concerning this modification was buried between two or more semiconductor chips 10 and each semiconductor chip 10.
[0090] (Gestalt of the 2nd operation) Drawing 4 (A) and drawing 4 (B) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation which applied this invention. With the gestalt of this operation, the formation method of a conductive member 28 differs from ****.
[0091] As shown in drawing 4 (A), with the gestalt of this operation, the 1st and 2nd semiconductor chips 11 and 13 are prepared. The 2nd through hole 24 which penetrates the 1st and 2nd semiconductor chips 11 and 13 according to the above-mentioned production process in the location of the electrode 14 of each semiconductor chip is formed. In the gestalt of this operation, a conductive member is prepared inside the 2nd through hole 24 in the 2nd semiconductor chip 13 in the solid condition. A conductive member may be a bump 32. A bump 32 may form from a pewter or gold.
[0092] A bump 32 is connected and formed in the electrode 14 (plating 16) of the 1st semiconductor chip 11. In detail, when carrying out the laminating of the 1st and 2nd semiconductor chips 11 and 13 and arranging them, a bump 32 is formed on the electrode 14 (plating 16) of the 1st semiconductor chip 11 which serves as the bottom beforehand. In the example to illustrate, the 1st semiconductor chip 11 is the semiconductor chip 10 with which conductive paste was filled up into the 2nd through hole 24 by the manufacture method in the gestalt of above-mentioned operation. A bump 32 forms in each electrode 14 of the 1st semiconductor chip 11. A bump 32 may do the laminating of the plurality and may form it so that it may illustrate. In this case, the laminating of the metal bumps of a different class may be carried out. For example, the laminating of the pewter bump may be carried out a golden bump and on it from an electrode 14 side. A bump 32 may form in the height more than the depth of the 2nd through hole 24 so that it may illustrate. A point (or all [a point]) forms a bump's 32 path at least in the magnitude which can enter into the 2nd through hole 24.
[0093] A bump's 32 formation method has plating, vacuum deposition, or the ball bump method, and may apply which method. Especially by the ball bump method which fuses a bonding wire and is formed in the shape of a ball, since it is easy to carry out the laminating of two or more bumps, it is easy to form the bump 32 who has the height more than

fixed (for example, height more than the depth of the 2nd through hole 24) and by whom the laminating was done.
[0094] By the bump 32, it is [electrical installation / of an electrode 14 and a conductive member 28 (conductive paste)] good in drawing in the 1st semiconductor chip 11. Since electrical installation of arrangement of the bump 32 for preparing in the 2nd semiconductor chip 13, and the electrode 14 and conductive member 28 in the 1st semiconductor chip 11 can be performed to coincidence according to this, simplification of a manufacturing process can be attained. After forming a bump 32, the bump 32 who prepared in the 1st semiconductor chip 11 is inserted in the 2nd through hole 24 in the 2nd semiconductor chip 13. A point may be located in the inside, without a bump's 32 penetrating the 2nd through hole 24, or penetrating the 2nd through hole 24. Moreover, a bump's 32 end face section may be located in the outside of the 2nd through hole 24 so that it may project from the field of the insulating material 22 in the 2nd semiconductor chip 13. Moreover, it can be made easy to enter a bump 32 into the 2nd through hole 24, when the above-mentioned taper 26 is given to the 2nd through hole 24 so that it may illustrate.
[0095] After inserting a bump 32 in the 2nd through hole 24, melting of the bump 32 may be carried out. In this case, as for a bump 32, being formed with a pewter is desirable. A conductive member can be made to fill up into the 2nd through hole 24 with carrying out melting of the bump 32. That is, the mechanical strength of the 2nd semiconductor chip 13 can be raised by filling the crevice between the 2nd through hole 24 in the 2nd semiconductor chip 13.
[0096] Or as long as it is the bump 32 who consists of gold etc., for example, the gestalt at the time of insertion may be left as it is, and a bump 32 may be formed inside the 2nd through hole 24 so that it may illustrate. Anyway, a conductive member can be certainly formed in the medial axis of the 2nd through hole 24.
[0097] As shown in drawing 4 (B), after carrying out the laminating of the 1st and 2nd semiconductor chips 11 and 13, in order to accumulate a semiconductor chip further, a bump 32 may be similarly formed in the 2nd semiconductor chip 13 of the maximum upper layer. By this, electrical installation of an electrode 14 and the conductive member in the 2nd through hole 24 (bump 32) can be planned in the 2nd semiconductor chip 13.
[0098] According to the above production process, while making it flow through both sides of the 1st and 2nd semiconductor chips 11 and 13 by the bump 32, the laminating of the 1st and 2nd semiconductor chips 11 and 13 can be carried out. Therefore, simplification of a manufacturing process can be attained.
[0099] as the 1st modification of the gestalt of this operation, the bump 32 is beforehand formed in another members (for example, substrate etc.) with the above-mentioned configuration, a bump 32 is inserted in the 2nd through hole 24 of a semiconductor chip 10 by putting a semiconductor chip 10 on said another member, and it is ** -- behind, a bump 32 may be removed from said another member, and a conductive member may be prepared in a semiconductor chip 10. That is, you may also insert a bump 32 in the 2nd through hole 24 of a semiconductor chip 10 with a replica method. In this case, if some bumps 32 have projected on the outside of the opposite side in the 2nd through hole 24 with the field in which the electrode 14 was formed, when carrying out a laminating to other semiconductor chips 10, the alignment of a semiconductor chip 10 becomes easy on the basis of the projecting portion. In addition, the configuration of the semiconductor device concerning this modification and its effect are as having already explained.
[0100] Drawing 5 is drawing showing some semiconductor devices concerning the 2nd modification of the gestalt of this operation. In this modification, the laminating of two or more semiconductor chips 60, 62, 64, and 66 is carried out, and the conductive member (for example, bump 32) of one of semiconductor chips is electrically connected to the portion which avoided the 2nd through hole 68 in the electrode 14 of a lower semiconductor chip in connection of an up-and-down semiconductor chip. In other words, in the plane view of one electrode 14, the portion which connects a conductive member, and the portion which carries out a opening by the 2nd through hole 68 are prepared so that it may not lap superficially.
[0101] According to this, before carrying out the laminating of two or more semiconductor chips 60-66, the bump 32 who connects with an electrode 14 electrically beforehand and prepares can be formed in the field of an electrode 14 (plating 16). That is, since it is not necessary to form a bump 32 on the 2nd through hole 68 in a lower semiconductor chip, electrical installation can be planned in the almost flat field of an electrode 14, and the condition of having been stabilized more.
[0102] Furthermore, a bump 32 does not need to connect with both other bumps 32, **, and coincidence which were prepared in the 2nd through hole 68 of the electrode 14 of a lower semiconductor chip, and a lower semiconductor chip electrically. That is, the production process which connects electrically the production process which connects electrically a bump 32 and the electrode 14 of a lower semiconductor chip, and the electrode 14 of a lower semiconductor chip and the bump 32 in the 2nd through hole 68 of a lower semiconductor chip can be made separate, and can be performed. By this, the defect of electrical installation can be lessened and the yield at the time of manufacture can be raised.
[0103] In addition, the semiconductor chip with which an electrode 14 and its electrode 14 were formed is electrically connected with the conductive member (for example, bump 32) prepared by penetrating with the electrical conducting

materials 70, such as **********. detailed -- an electrical conducting material 70 -- an electrode 14 (plating 16) and a conductive member (for example, bump 32) -- a wrap -- both electrical installation can be planned by preparing like.

[0104] The gestalt of others in this modification can apply the contents of the arbitration by which a laminating is carried out up and down among two or more semiconductor chips 60-66 above-mentioned [two] as the 1st and 2nd semiconductor chips. Moreover, the manufacture method of the semiconductor device in this modification is as having already explained.

[0105] (Gestalt of the 3rd operation) Drawing 6 (A) and drawing 6 (B) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 3rd operation which applied this invention. With the gestalt of this operation, the gestalt of the 2nd through hole 25 differs from ****.

[0106] As shown in drawing 6 (A), with the gestalt of this operation, a taper 27 attaches and forms the 2nd through hole 25. In detail, the taper 27 which becomes small is attached and formed as the 2nd through hole 25 is separated from the electrode 14 of a semiconductor chip 10. The 2nd through hole 25 may glare and form a laser beam from the electrode 14 side of a semiconductor chip 10, or with it, from the opposite side, it is irradiated and it may form it. In addition, the 2nd other gestalten and formation methods of a through hole 25 are as given in ****.

[0107] Drawing 6 (B) is drawing which has the semiconductor chip 10 with which the 2nd above-mentioned through hole 25 was formed and in which showing the semiconductor device 5 of stack structure. A conductive member 34 is formed so that the 2nd through hole 25 may pass along the medial axis. The conductive member 34 is buried by the example to illustrate by the 2nd through hole 25. For example, a solid bump may be inserted in the 2nd through hole 25, and a conductive member 34 may be filled up into the 2nd through hole 25 with the bump fusing, and may be formed by solidifying again. In this case, a bump may be a pewter bump. A part of solidified conductive member 34 may be projected from opening of a side with the small path in the 2nd through hole 25. According to this, the omission stop of a conductive member 34 can be planned with the taper 27 given to the inside of the 2nd through hole 25. a conductive member 34 can be made hard to escape from from the 2nd through hole 25, when the portion which projects outside is resembled from opening of the inside of the 2nd through hole 25, and the minor diameter of the 2nd through hole 25 and a conductive member 34 is formed in one in detail so that it may illustrate. In addition, other configurations and effects may be the same as that of ****.

[0108] Although the manufacture method of the semiconductor device mentioned above was performed to the semiconductor chip 10, as shown in drawing 7 , it may perform this to a semiconductor wafer 40 (semiconductor device). A semiconductor wafer may perform an above-mentioned production process using that by which grinding was thinly carried out to the thickness of a basis. After a semiconductor wafer 40 carries out the laminating of the plurality up and down with the application of the above-mentioned manufacture method, the dicing of it may be carried out to each semiconductor chip 10. In detail, two or more semiconductor wafers 40 which come to carry out a laminating may be cut in the vertical direction, and may be divided into the semiconductor chip 10 of stack structure. Or before the production process which carries out a laminating up and down, an above-mentioned production process is performed to a semiconductor wafer 40, after that, the laminating of each semiconductor chip 10 which carried out dicing may be carried out, and the semiconductor device of stack structure may be manufactured. Thus, a semiconductor device can be efficiently manufactured by performing an above-mentioned production process to a semiconductor wafer 40. In addition, about a semiconductor wafer, this invention is applicable also to what performed relocation wiring processing to the semiconductor wafer called Wafer CSP, and the thing which established stress relaxation structure.

[0109] The circuit board 50 which mounted the semiconductor device 7 concerning the gestalt of the operation which applied this invention in drawing 8 is shown. It is common to the circuit board 50 to use organic system substrates, such as for example, a glass epoxy group board. Those electric flows are aimed at by being formed in the circuit board 50 so that the circuit pattern 52 which consists of copper etc. may serve as a desired circuit, and connecting mechanically those circuit patterns 52 and pewters 30 of a semiconductor device 7.

[0110] Or the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation is applied, for example, you form the bumps 32, such as a ball bump, in the circuit pattern 52 of the circuit board 50 beforehand, and may also insert a bump 32 in the 2nd through hole 24 by carrying on it a semiconductor chip 10 (one or two or more semiconductor chips 10 which come to carry out a laminating).

[0111] Or it is [electrical installation / with the circuit board 50] good in drawing by the external terminal which mounts in the substrate (INTAPOZA) which is not illustrated for mounting a semiconductor device 7 in the circuit board 50, and is formed in a substrate.

[0112] And the cellular phone 200 is shown in the note type personal computer 100 and drawing 10 at drawing 9 as electronic equipment which has a semiconductor device concerning the gestalt of the operation which applied this

invention.

[0113] In addition, the "semiconductor chip" of the gestalt of operation mentioned above can be transposed to a "electronic device", and electronic parts can also be manufactured. As electronic parts manufactured using such an electronic device, there is for example, a light corpuscle child, a resistor, a capacitor, a coil, an oscillator, a filter, a temperature sensor, a thermistor, a varistor, volume, or a fuse.

[Translation done.]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] A manufacture method of a semiconductor device including the 2nd production process established so that a field containing the 1st production process which forms the 1st through hole penetrated in a location of said electrode to a semiconductor device which has an electrode, and the inside of said 1st through hole may be equipped with the 2nd through hole which penetrates said insulating material for an insulating material, and the 3rd production process which prepares a conductive member by the inside of said 1st through hole in the 2nd through hole which penetrates said insulating material at least.
[Claim 2] A manufacture method of a semiconductor device which includes further a production process which carries out the laminating of two or more semiconductor devices manufactured by method according to claim 1, and connects said up-and-down semiconductor device electrically through said conductive member.
[Claim 3] A manufacture method of a semiconductor device characterized by providing the following The 1st production process which forms the 1st through hole penetrated in a location of said electrode to the 1st and 2nd semiconductor devices which have an electrode The 2nd production process prepared in a field containing the inside of said 1st through hole so that it may have the 2nd through hole which penetrates said insulating material for an insulating material, and the 3rd production process which accumulates said 1st and 2nd semiconductor devices while connecting electrically, preparing a conductive member at said electrode of said 1st semiconductor device and inserting said conductive member in said 2nd through hole in said 2nd semiconductor device
[Claim 4] A manufacture method of a semiconductor device of covering and establishing a field opposite to a field in which said electrode in said semiconductor device was formed in said insulating material at said 2nd production process in a manufacture method of a semiconductor device a publication in either of claim 1 to claims 3.
[Claim 5] It is the manufacture method of a semiconductor device which connects said conductive member and said electrode electrically by said insulating material's consisting of resin in a manufacture method of a semiconductor device according to claim 4 of quoting either claim 2 or claim 3, heating [said two or more semiconductor devices] lamination and said resin for said resin as adhesives, and making hardening contraction of said resin complete.
[Claim 6] A manufacture method of a semiconductor device of heating said resin and making the adhesive strength discovering in a manufacture method of a semiconductor device according to claim 5 before sticking said two or more semiconductor devices.
[Claim 7] It is the manufacture method of a semiconductor device of said insulating material consisting of resin, being said 2nd production process, applying said resin in a manufacture method of a semiconductor device given in either of claim 1 to claims 6, and preparing.
[Claim 8] A manufacture method of a semiconductor device which forms said 2nd through hole so that said 1st through hole may be buried to either of claim 1 to claims 7 at said 2nd production process, said insulating material may be prepared in it at it in a manufacture method of a semiconductor device a publication and said insulating material may be penetrated with a path smaller than said 1st through hole inside said 1st through hole.
[Claim 9] It is the manufacture method of a semiconductor device of said conductive member being conductive paste in a manufacture method of a semiconductor device given in either of claim 1 to claims 8, being said 3rd production process, and making said 2nd through hole filling up with said conductive paste.
[Claim 10] It is the manufacture method of a semiconductor device of said conductive member being a bump in a manufacture method of a semiconductor device according to claim 3, being said 3rd production process, and inserting said some of bumps [at least] in said 2nd through hole in said 2nd semiconductor device.
[Claim 11] It is the manufacture method of a semiconductor device that plurality comes to carry out the laminating of said bump in a manufacture method of a semiconductor device according to claim 10.
[Claim 12] A manufacture method of a semiconductor device of carrying out melting of said bump and making said

2nd through hole filled up with her after said 3rd production process in a manufacture method of a semiconductor device according to claim 10 or 11.

[Claim 13] A manufacture method of a semiconductor device which attaches and forms a taper which becomes small as said electrode of said semiconductor device is approached in said 2nd through hole in a manufacture method of a semiconductor device given in either of claim 1 to claims 12.

[Claim 14] A manufacture method of a semiconductor device which attaches and forms a taper which becomes small as said 2nd through hole is separated from said electrode of said semiconductor device in a manufacture method of a semiconductor device given in either of claim 1 to claims 12.

[Claim 15] It sets to a manufacture method of a semiconductor device given in either of claim 1 to claims 14, and is the manufacture method of a semiconductor device of said 1st through hole or said 2nd through hole which forms either by laser beam at least.

[Claim 16] A manufacture method of a semiconductor device which irradiates said laser beam in a manufacture method of a semiconductor device according to claim 15 from a field opposite to a field in which said electrode of said semiconductor device was formed.

[Claim 17] A semiconductor device which either of claim 1 to claims 16 comes to manufacture by the manufacture method of a semiconductor device a publication.

[Claim 18] A semiconductor device containing a semiconductor device which has an electrode and by which a through hole was formed in a location of said electrode, an insulating material prepared in a field including an inside of said through hole, and a conductive member prepared so that it might pass along a medial axis of said through hole.

[Claim 19] It is the semiconductor device which said conductive member buries said through hole in a semiconductor device according to claim 18, and it comes to prepare.

[Claim 20] It is the semiconductor device which it comes to give a taper which becomes small as said through hole approaches said electrode of said semiconductor device in a semiconductor device according to claim 18 or 19.

[Claim 21] It is the semiconductor device which it comes to give a taper which becomes small as said through hole separates from said electrode of said semiconductor device in a semiconductor device according to claim 18 or 19.

[Claim 22] It is the semiconductor device which said insulating material covers a field opposite to a field in which said electrode in said semiconductor device was formed while exposing said conductive member in a semiconductor device given in either of claim 18 to claims 21, and it comes to prepare.

[Claim 23] A field in which said electrode [in / on a semiconductor device given in either of claim 18 to claims 22 and / in said conductive member / said semiconductor device] was formed is a semiconductor device which it comes to project on the outside of said through hole in the opposite side in a part.

[Claim 24] A semiconductor device to which the laminating of the semiconductor device of a publication is carried out to either of claim 18 to claims 23, and said conductive member comes to connect said up-and-down semiconductor device electrically.

[Claim 25] The circuit board by which a semiconductor device of a publication was carried in either of claim 17 to claims 24.

[Claim 26] Electronic equipment which has a semiconductor device of a publication in either of claim 17 to claims 24.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 (A) - drawing 1 (C) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 1st operation which applied this invention.
[Drawing 2] Drawing 2 (A) - drawing 2 (C) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 1st operation which applied this invention.
[Drawing 3] Drawing 3 is drawing explaining the manufacture method of the semiconductor device concerning the modification of the gestalt of the 1st operation which applied this invention.
[Drawing 4] Drawing 4 (A) and drawing 4 (B) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation which applied this invention.
[Drawing 5] Drawing 5 is drawing showing some semiconductor devices concerning the modification of the gestalt of the 2nd operation which applied this invention.
[Drawing 6] Drawing 6 (A) and drawing 6 (B) are drawings showing the manufacture method of the semiconductor device concerning the gestalt of the 3rd operation which applied this invention.
[Drawing 7] Drawing 7 is drawing showing the manufacture method of the semiconductor device concerning the gestalt of the operation which applied this invention.
[Drawing 8] Drawing 8 is drawing showing the circuit board in which the semiconductor device concerning the gestalt of the operation which applied this invention was mounted.
[Drawing 9] Drawing 9 is drawing showing the electronic equipment which has a semiconductor device concerning the gestalt of the operation which applied this invention.
[Drawing 10] Drawing 10 is drawing showing the electronic equipment which has a semiconductor device concerning the gestalt of the operation which applied this invention.
[Description of Notations]
10 Semiconductor Chip
14 Electrode
18 1st through Hole
22 Insulating Material
24 2nd through Hole
25 2nd through Hole
26 Taper
27 Taper
28 Conductive Member
32 Bump
34 Conductive Member
40 Semiconductor Wafer

[Translation done.]

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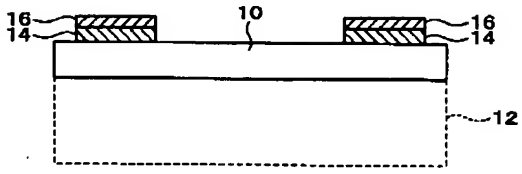
DRAWINGS

[Drawing 1]

(A)



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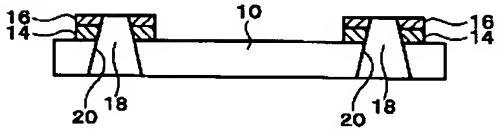

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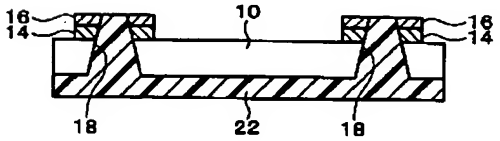
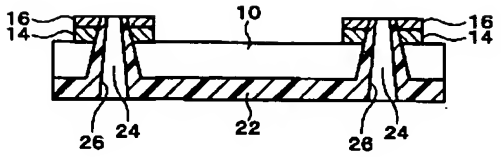


[Drawing 2]

(A)



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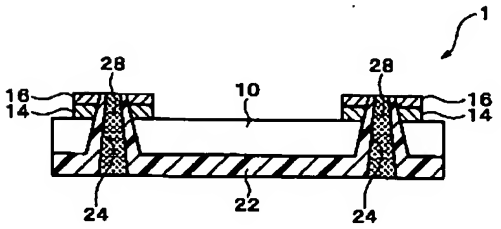

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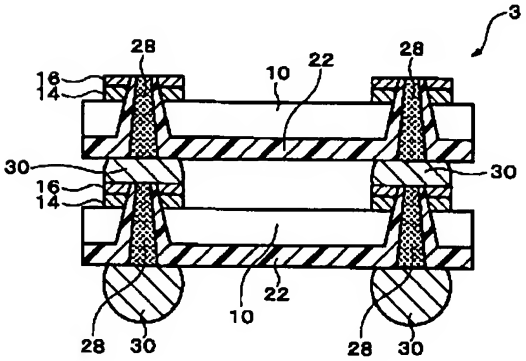

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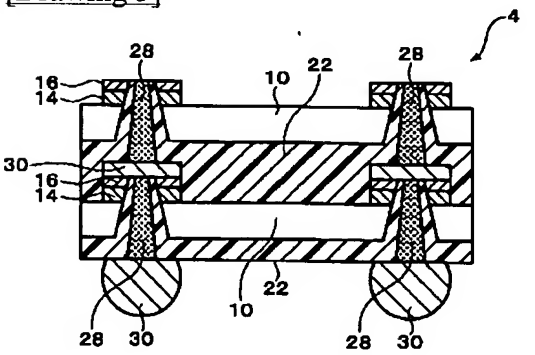

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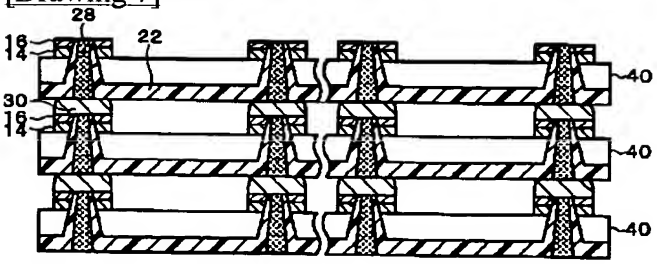
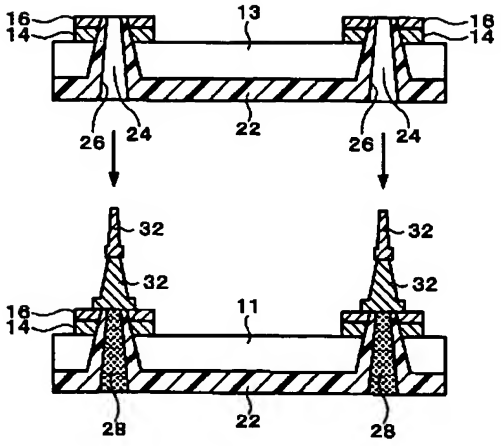


[Drawing 4]

(A)



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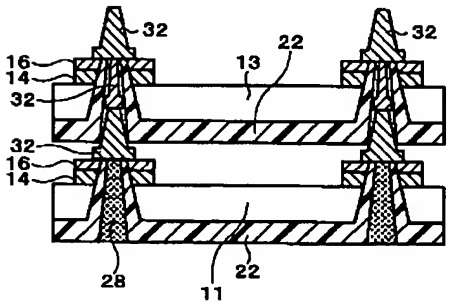

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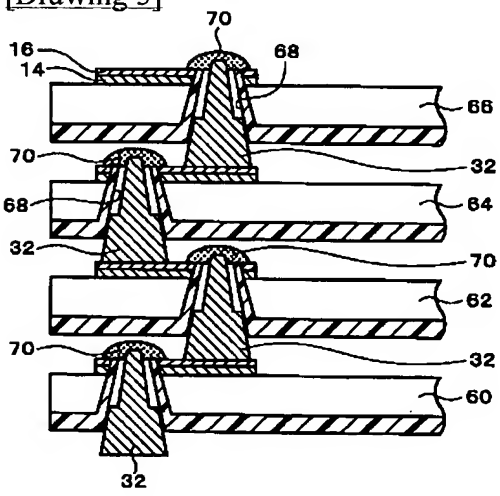
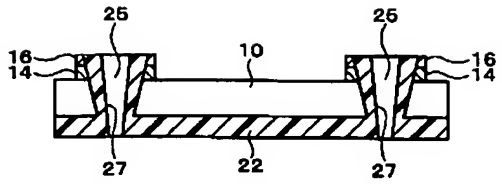


[Drawing 6]

(A)



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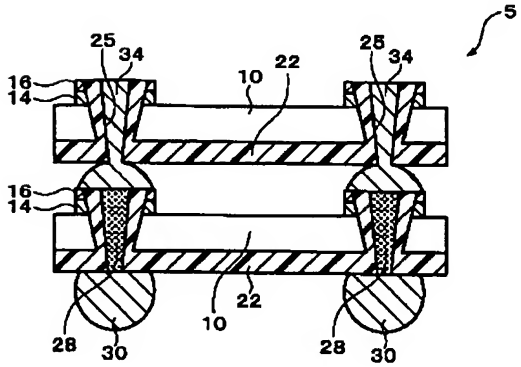

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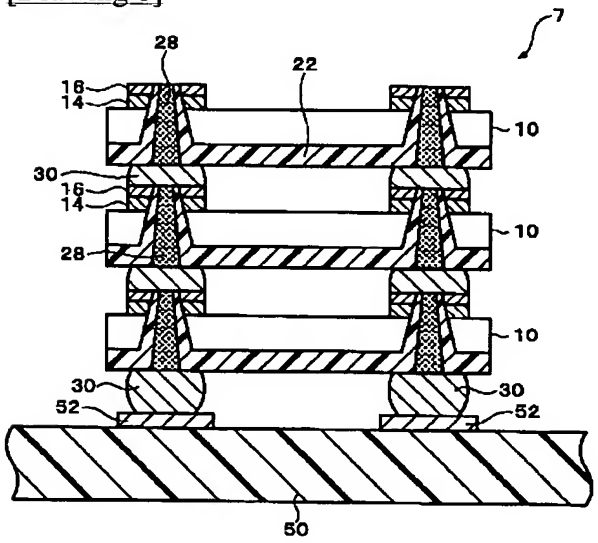

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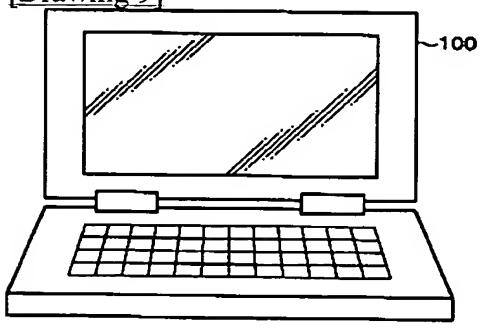
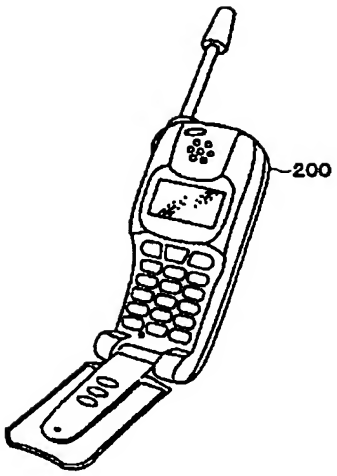


[Drawing 10]



[Translation done.]